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17EC34

Third Semester B.E. Degree Examination, Aug./Sept.2020
Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Construct a truth table and write the Boolean output for a single output 2 which is to be true when the input variables a and b are true and when b is false, but a and c are true. Implement the Boolean expression using gates. **(04 Marks)**

b. Convert the given Boolean function :

(i) $f_1 = f(a, b, c, d) = (a + \bar{b} + c)(\bar{a} + d)$ into maxterm canonical form

(ii) $f_2 = f(w, x, y, z) = \bar{w}x + y\bar{z}$ into minterm canonical form. **(08 Marks)**

c. Identify the prime implicants and essential prime implicants for the following expression.

(i) $f(a, b, c, d) = \Sigma(1, 5, 7, 8, 9, 10, 11, 13, 15)$

(ii) $f(a, b, c, d) = \pi(0, 2, 3, 8, 9, 10, 12, 14)$ **(08 Marks)**

OR

2 a. Find the minimal sum and minimal product for the following Boolean function using Kmap.

$Y = f(u, v, w, x) = \Sigma(1, 5, 7, 9, 13, 15) + \Sigma d(8, 10, 11, 14)$ **(08 Marks)**

b. Simplify the following expression using Quine McCluskey method and find the minimal sum using PI reduction table.

$f(a, b, c, d) = \Sigma(2, 3, 4, 5, 13, 15) + \Sigma d(8, 9, 10, 11)$ **(12 Marks)**

Module-2

3 a. Design a circuit that will find the 2′s complement of a three bit binary number. Draw the logic diagram for the reduced equations. **(08 Marks)**

b. Draw the logic diagram, function table and IEEE logic symbol of a 2 to 4 line decoder in 74139 IC. Realize the Boolean function $X = f(a, b, c) = (0, 3, 5, 6)$ using 74139. **(12 Marks)**

OR

4 a. Realize the following Boolean function using 4:1 multiplexer with a, b as select lines.

$f(a, b, c, d) = \Sigma(0, 3, 4, 5, 7, 9, 13, 15)$ **(06 Marks)**

b. Design a BCD adder using 7483. **(06 Marks)**

c. Design a two bit magnitude comparator. **(08 Marks)**

Module-3

5 a. Explain the working of a SR latch as a switch debouncer with necessary circuit and timing diagram. **(06 Marks)**

b. Explain the working of master slave JK flip flop with the help of a logic diagram, function table, logic symbol and timing diagram. **(10 Marks)**

c. Explain race around condition and how it is overcome. **(04 Marks)**

OR

6 a. Explain with timing diagram for (i) SR flip flop and (ii) D flip flop. **(06 Marks)**

b. Derive the characteristic equation for JK and T flip flop. **(06 Marks)**

c. With a neat logic diagram, explain the working of positive edge triggered D flip flop. Also draw the timing diagram. **(08 Marks)**

Module-4

7 a. Design a register using four multiplexer and positive edge triggered D flip flop having the behavior specified in the table below.

S_1	S_0	Register operation
0	0	Hole
0	1	Synchronous clear
1	0	Complement contents
1	1	Circular shift right.

(08 Marks)

b. Illustrate the operation of 4-bit binary ripple counter using positive edge triggered D flip flop without a count enable line. **(08 Marks)**

c. Design a MOD 7 twisted ring counter. Write the logic diagram and counting sequence. **(04 Marks)**

OR

8 a. Design a Mod 6 counter whose counting sequence is 000, 001, 100, 110, 111, 101, 000…. by using positive edge triggered JK flip flop. **(10 Marks)**

b. Show how an 8 bit synchronous binary counter can be constructed from two 4 bit synchronous binary counters. **(04 Marks)**

c. Explain PIPO and PISO shift register with relevant logic diagrams. **(06 Marks)**

Module-5

9 a. Explain the Mealy model and Moore model of a clocked synchronous sequential network. **(08 Marks)**

b. Give the logic diagram shown in Fig.Q9(b).
(i) Derive the excitation and output equations.
(ii) Write the next state equations
(iii) Construct a state transition table
(iv) Draw the state diagram.

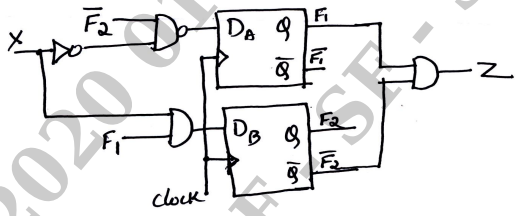

Fig.Q9(b) **(12 Marks)**

OR

10 a. Construct mealy state diagram that will detect input sequence 10110, when input pattern is detected, Z is asserted high. Give state diagram for each state. **(10 Marks)**

b. Design a sequential circuit for a state diagram shown in Fig.Q10(b) using JK flip flop.

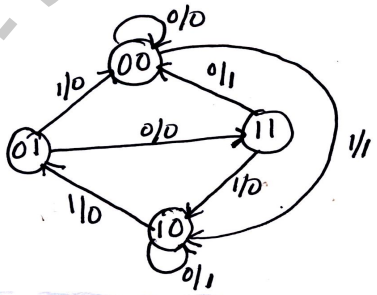

Fig.Q10(b) **(10 Marks)**

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